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Utilizing Low-Threshold Voltages for Increased Battery Life

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Decreasing power consumption and extending the battery life is the goal of every design engineer working on portable electronic products. Battery technology has progressed very slowly, so designers of portable products pay a lot of attention to power management to improve battery life. For many years, semiconductor manufacturers targeting power management applications have struggled to keep pace with the demands of the end system users. An increasing number of portable electronic products, with heightened levels of functionality, demand peak performance and challenge designers to achieve the highest efficiency possible within the device's physical bounds. Although the battery industry has been making efforts to develop alternative battery technologies with a higher energy capacity than that of conventional Nickel-Cadmium (NiCd) batteries, it is nowhere close to delivering the power requirements of new-generation portable devices. Therefore, portable applications have led to innovative developments in low-power circuit designs so that design engineers can ensure that the end system utilizes battery resources as efficiently as possible. Components are a major part of the power budget in portable devices, and obviously, to keep up with that demand, semiconductor component manufacturers continue to drive innovation to help reduce power consumption in portable devices.

Taking a cellular phone as an example, reducing the operating voltage of the major components of the handset, such as the analog and digital baseband chips, is one way of reducing power consumption. When maximum performance from a DSP or microprocessor isn't necessary, the core supply voltage can be lowered to operate at a reduced clock frequency. More and more new-generation low-power applications are implementing this technique to maximize system power conservation. The formula $\mathbf{PC \sim (V_C)^2.F}$ describes the power consumption of a DSP core, where **PC** is core power consumption, $\mathbf{V_C}$ is core voltage, and **F** is the core clock frequency. Lowering the internal clock frequency can reduce the power consumption; lowering the core supply voltage can reduce it even further.

Many designers following this simple approach have moved to using 2.7 V or even 1.8 V as an operating voltage. Although it would be highly desirable to operate the chips at voltages even lower than 1.8 V, lack of components "safely" operating at lower voltages have so far made this an elusive goal. While these design parameters will provide users with a compelling and functional package, they also will impose stringent requirements on power management circuitry. This is forcing manufacturers and designers to develop new architectures that can deliver more power with greater efficiency for increased battery life at about the same level of cost.

HOW ADVANCED SILICON AND PACKAGING TECHNOLOGY CAN HELP

While there are many design factors that affect the performance of new power-hungry portable devices, this article focuses on power MOSFETs — the most common power switches for low-voltage applications — to illustrate the impact of the latest silicon

breakthroughs on increasing power requirements. In order to explain the impact of these advancements, it helps to understand some critical parameters of power MOSFETs.

Channel on-resistance ($r_{DS(on)}$) is controlled by the electric field present across and along the channel. Channel resistance is mainly determined by the gate-to-source voltage difference. When V_{GS} exceeds the threshold voltage ($V_{GS(th)}$), the FET starts to turn on. Many operations call for switching a point to ground. The resistance of a power MOSFET channel is related to its physical dimensions by the formula **R=ρL/A**, where **ρ** is resistivity, **L** is the length of the channel, and **A** is W x T, the cross-sectional area of the channel.

In the usual FET structure, L and W are fixed by device geometry, while channel thickness T is the distance between the depletion layers. The position of the depletion layer can be varied either by the gate-source bias voltage or by the drain-source voltage. When T is reduced to zero by any combination of V_{GS} and V_{DS}, the depletion layers from the opposite sides come in contact, and the incremental channel resistance ($r_{DS(on)}$) approaches infinity.

Figure 1 explains the $r_{DS(on)}$ versus V_{GS} characteristic. Region I corresponds to the condition when the accumulative charge is not sufficient to cause an inversion. Region II corresponds to the condition where sufficient charge is present to invert a portion of the p region, forming the channel, but not enough that the “space charge” effect is important. Region III corresponds to the charge-limited condition where $r_{DS(on)}$ does not change appreciably as the gate-body potential is raised.

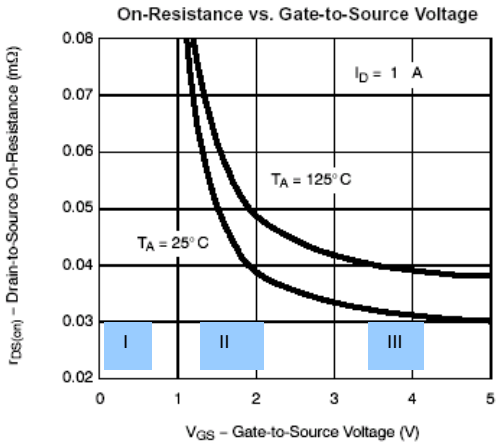

Figure 1: $r_{DS(on)}$ versus V_{GS} characteristic

The threshold voltage ($V_{GS(th)}$) is a parameter used to describe how much voltage is needed to initiate the channel conduction. V_{GS} controls the magnitude of the saturated I_D, with increases in V_{GS} resulting in lower values of constant I_D, and smaller values of V_{DS} necessary to reach the “knee” of the curve (Figure 2).

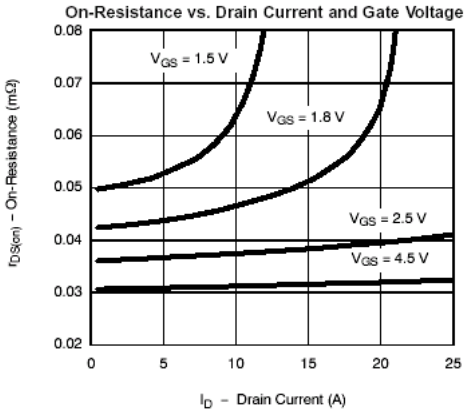

Figure 2: $r_{DS(on)}$ versus Id for different gate voltages (Source: Vishay Siliconix Si8419DB datasheet)

High-speed performance and low-power operation can be achieved by utilizing low-threshold voltage transistors. By using low-threshold power MOSFETs in a signal path, the supply voltage (V_{DD}) can be lowered to reduce the switching power dissipation without affecting the performance. That's why, to address the ever-increasing demand to minimize power consumption and increase battery life, many of the ASICs found in portable electronics systems are designed to operate at core supply voltages around 1.5 V. Until now, however, the lack of power MOSFETs with guaranteed turn-on operation at such low voltages has made it difficult for designers to take advantage of these sub-1.8-V voltages without the use of level-shifting circuitry, which adds complexity while increasing power consumption. Vishay Siliconix is addressing this problem with a breakthrough family of power MOSFETs that are the industry's first with guaranteed on-resistance ratings at 1.5-V.

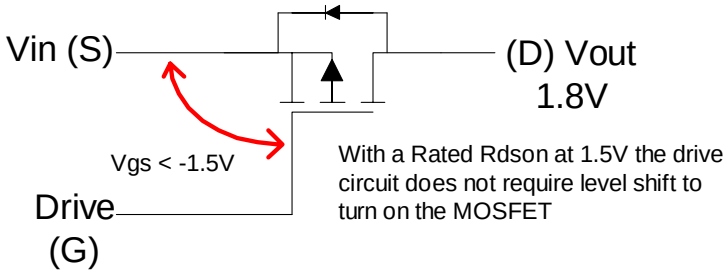

Figure 3. Reducing the $V_{GS(th)}$ point allows the driver voltage to turn on the switch from a lower-output voltage, reducing the need for a level shifting.

Historically, a threshold voltage no lower than 1.8 V was needed to accommodate the negative temperature coefficient of the threshold point that occurs in all power MOSFETs. For operation at 125 °C (which is quite possible in portable applications), the existing MOSFET designs had to maintain the MOSFET threshold high in order to prevent the MOSFET from turning itself on despite a V_{GS} of 0 V being applied.

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When it comes to portable devices and cell phones in particular, there is no end in site to the demand for new multimedia features. For designers struggling to deliver higher data capabilities while juggling the unique power requirements of next-generation portable devices, however, there is little question that the advanced silicon and packaging technology of today's power MOSFETs may bring the required edge in delivering power efficiency, ultra-compact size, and low cost required to make these multimedia phones a reality.